REMARKS

Claims 1-26 are pending in the above-identified application and stand rejected. Applicants, having amended the application, respectfully request reconsideration.

Amendments to the Specification and Figures

Applicants have made numerous changes to the specification and figures to fix obvious typographical and grammatical errors. The examiner suggested many of the changes. Applicants appreciate the examiner's attention to detail. No new matter is added.

Priority

The examiner noted that applicants have yet to send in a certified copy of one of the priority documents, a PCT application with docket number MBHB00-167-B. Applicants will order and forward a certified copy of that application.

Rejections under 35 U.S.C. §103

Claims 1-26 stand rejected under §103. All of claims 1-26 are cancelled, rendering those rejections moot.

New Claims

This amendment introduces new claim 27-41, including independent claims 27, 35, and 39. These claims make reference to elements detailed in U.S. Patent No. 6,772,351 (the '351 patent). The '351 is a parent of the present application, and was incorporated by reference at page 2, lines 3-9, as U.S. Patent Application Serial No. 09/654,643. In accordance with MPEP 608.01(p), both essential and non-essential subject material may be incorporated into a patent application by reference to an issued U.S. Patent. It is therefore proper to look to the incorporated patent for support for the new claims. As noted below, Figure 13 of the present application combined with Figures 9A and 10 from the '351 are collectively a system in support of the new claims. These three figures are reproduced below for ease of review.

Claims 27-34

Claim 27 recites a system that includes a multi-PAM output driver, a current-calibration circuit, and a multi-level voltage generator. The '351 patent supports both the multi-PAM output driver and the current-calibration circuit, while the present application adds to these the multi-level voltage generator.
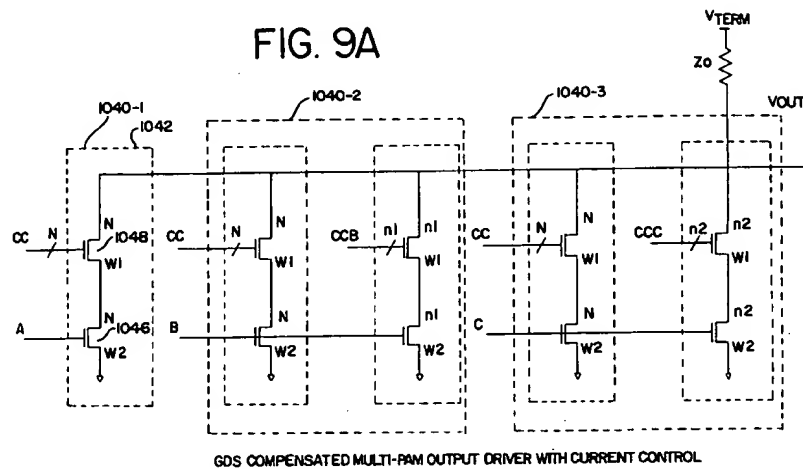
FIG. 9A

GDS COMPENSATED MULTI-PAM OUTPUT DRIVER WITH CURRENT CONTROL

Fig. 9A of '351 patent

Figure 9A of the '351 patent, shown above, depicts a multi-PAM output driver with current-calibration ports CC, CCB, and CCC. The corresponding calibration "bits" come from the calibration circuit in Fig. 10 of the '351 patent, which is reproduced below.

CIRCUIT FOR CALIBRATING THE GDS COMPENSATED
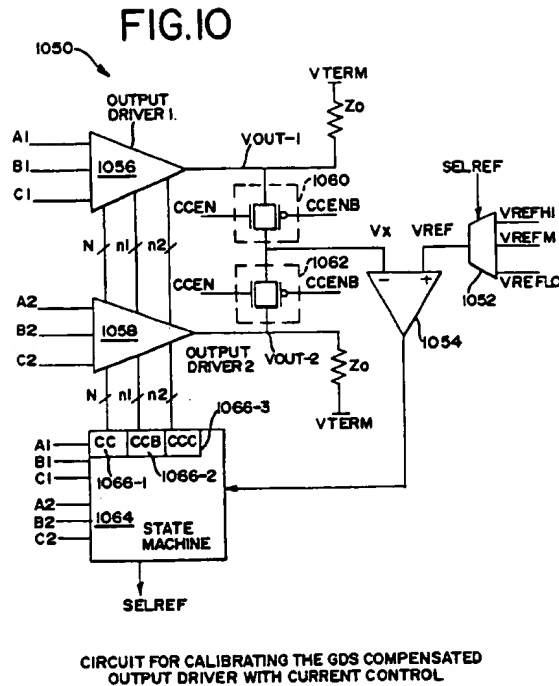OUTPUT DRIVER WITH CURRENT CONTROL

Fig. 10 of '351 patent

The '351 patent details how the calibration circuitry 1050 of Fig. 10 generates the current-calibration signals CC, CCB, and CCC for application to the corresponding ports of the driver depicted in Fig. 9A. In summary, state machine 1064 of Fig. 10 generates the CC, CCB, and CCC signals.

The '351 patent details how the calibration circuitry 1050 of Fig. 10 develops the current-calibration signals CC, CCB, and CCC using a number of reference voltages V_{REFHI}, V_{REFM} and V_{REFLO}. These reference voltages and their corresponding nodes are depicted at the far right of Fig. 10 of the '351 patent as inputs to a multiplexer 1052. The present application is directed to methods and circuits for adjusting reference voltages V_{REFHI}, V_{REFM} and V_{REFLO} to achieve desired levels of equalization and cross-talk cancellation. As shown in applicants' Fig. 13, reproduced below, a 4-PAM voltage generator 1000 generates the reference voltages V_{REFHI}, V_{REFM} and V_{REFLO} for application to the like-named terminals of e.g. the calibration circuitry 1050 detailed in Fig. 10 of the '351 patent. Though not shown here, applicants Fig. 14 likewise shows a voltage generator that develops reference voltages V_{REFHI}, V_{REFM} and V_{REFLO}.

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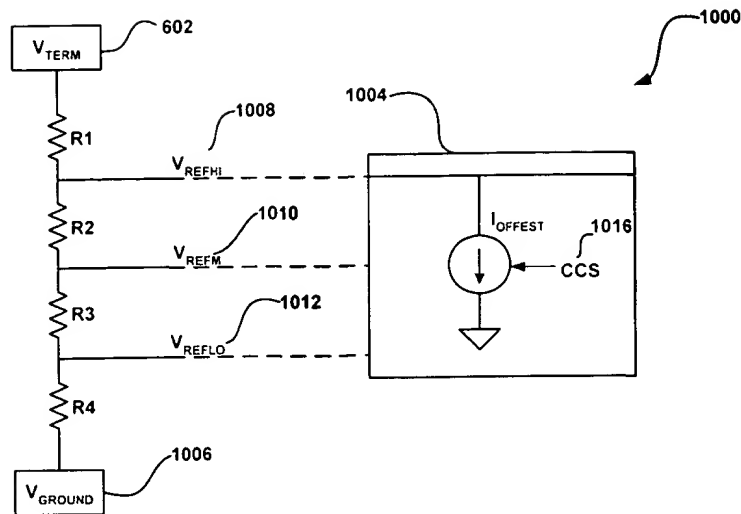
FIGURE 13

Fig. 13 of the Present Application

The above-reproduced figures, along with the associated text, describe a system in support of new claim 27. The manner in which the multi-PAM transmitter is calibrated using an offset current is neither taught nor suggested in the cited references or elsewhere, to Applicants' knowledge. Claim 27 is therefore believed to be allowable.

Claims 28-34 depend from claim 27, and are therefore believed to be allowable for at least the same reasons as claim 27.

Claims 35-38

Claim 35 is directed to "current-calibration circuitry for a multi-PAM output driver." The claimed circuitry includes a current-calibration circuit supported by the above-reproduced Figure 10 of the '351 patent and a multi-level voltage generator supported by Figure 13 of the present application. The circuits of those two figures share voltage-reference terminals V_{REFHI}, V_{REFM} and V_{REFLO}, together creating support for the claimed current-calibration circuitry. Claims 36-38 each depend upon claim 35, and consequently include the limitations of that base claim.
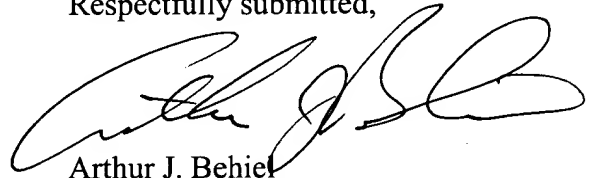
Claims 39-41

Claim 39 recites a method of calibrating a multi-PAM output driver. The method

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includes "dividing a reference voltage into a plurality of multi-PAM reference voltages" in the manner discussed in connection with Fig. 13, and additionally includes a shifting of logic states that is noted in the application e.g. at page 25, beginning at line 13.

CONCLUSION

In light of the foregoing remarks and amendments, the pending claims are in condition for allowance; accordingly, applicants respectfully request a notice of allowance. If the examiner's next action is other than allowance of the pending claims, the Examiner is requested to call applicants' attorney at (925) 621-2113.
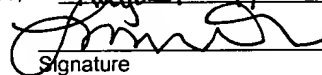
Respectfully submitted,

Arthur J. Behiel
Reg. No. 39,603

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on _August 19, 2005_.

Laurie Moreno
Name   Signature

In the Figures

Please amend the figures as indicated in red ink on the attached sheets. Applicants have also included replacement pages to be used should the examiner enter the amendments. Thus, no new matter is added.
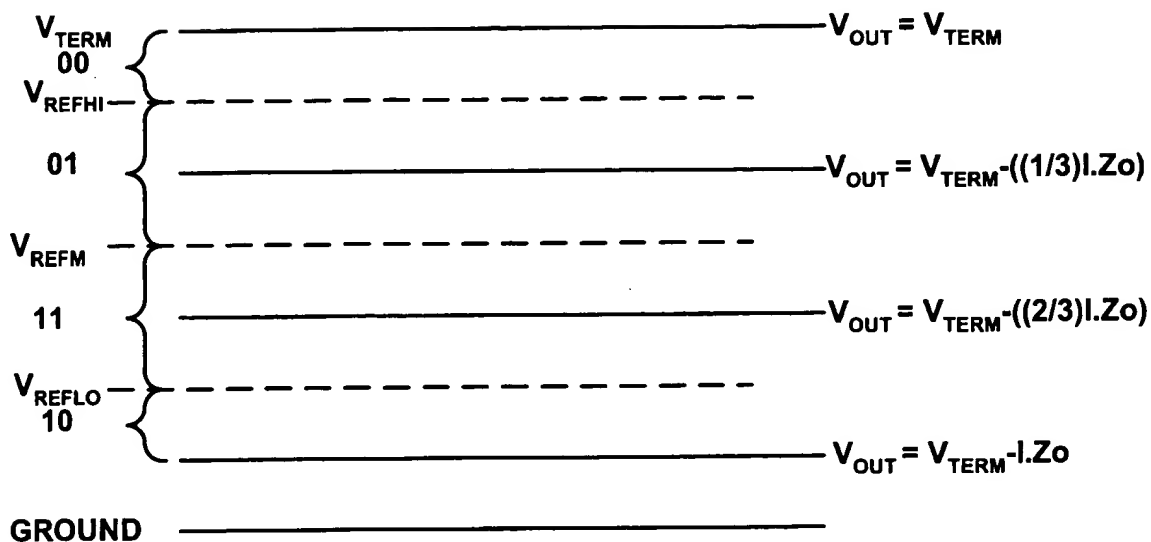
FIGURE 2 (Prior Art)

V_{TERM}
00
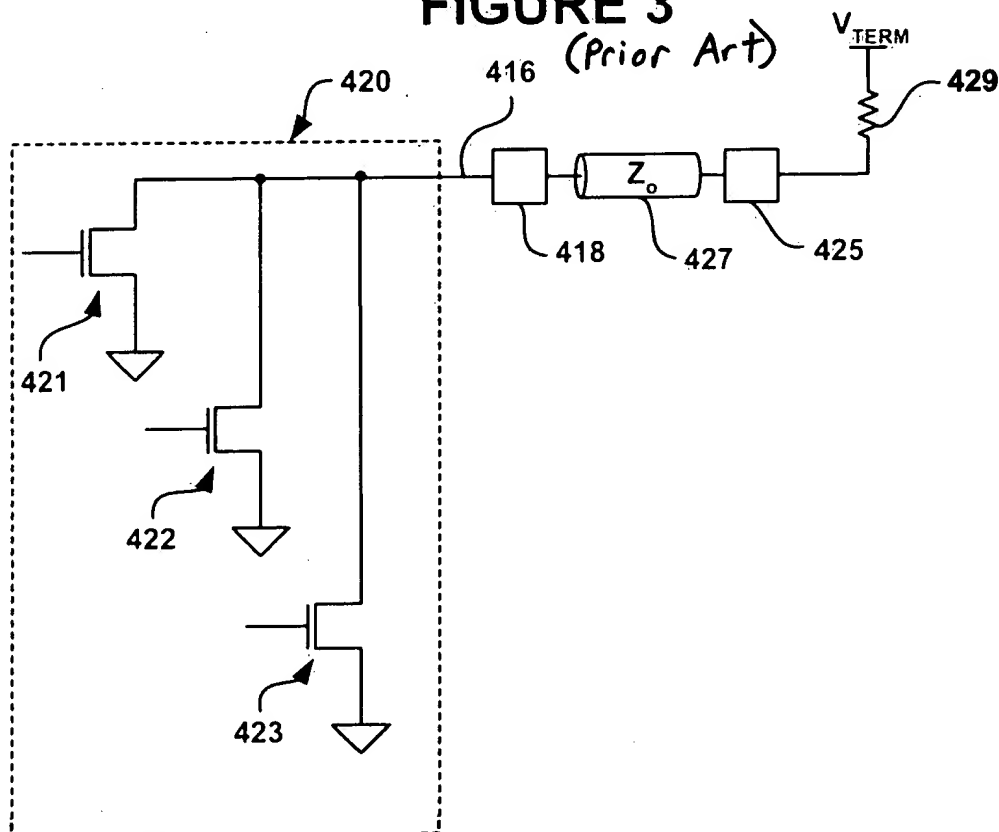$V_{OUT} = V_{TERM}$

V_{REFHI}

01
$V_{OUT} = V_{TERM} - ((1/3)I.Zo)$

V_{REFM}

11
$V_{OUT} = V_{TERM} - ((2/3)I.Zo)$

V_{REFLO}
10
$V_{OUT} = V_{TERM} - I.Zo$

GROUND

FIGURE 3
(Prior Art)

V_{TERM}

420   416   429

421

422

423

418   Z_o 425

427

FIGURE 4
(Prior Art)

500

V_{TERM} 502

V_{REF} 504

506

508

R1

R2

R3

510

512

514

V_{REFHI}

V_{REFM}

V_{REFLO}

FIGURE 5
(Prior Art)

600

V_TERM — 602

R1

— V_REFHI

R2

— V_REFM

R3

— V_REFLO

R4

FIGURE 6

- - - - 00

- - - - 00

- - - - 00

01

10

11
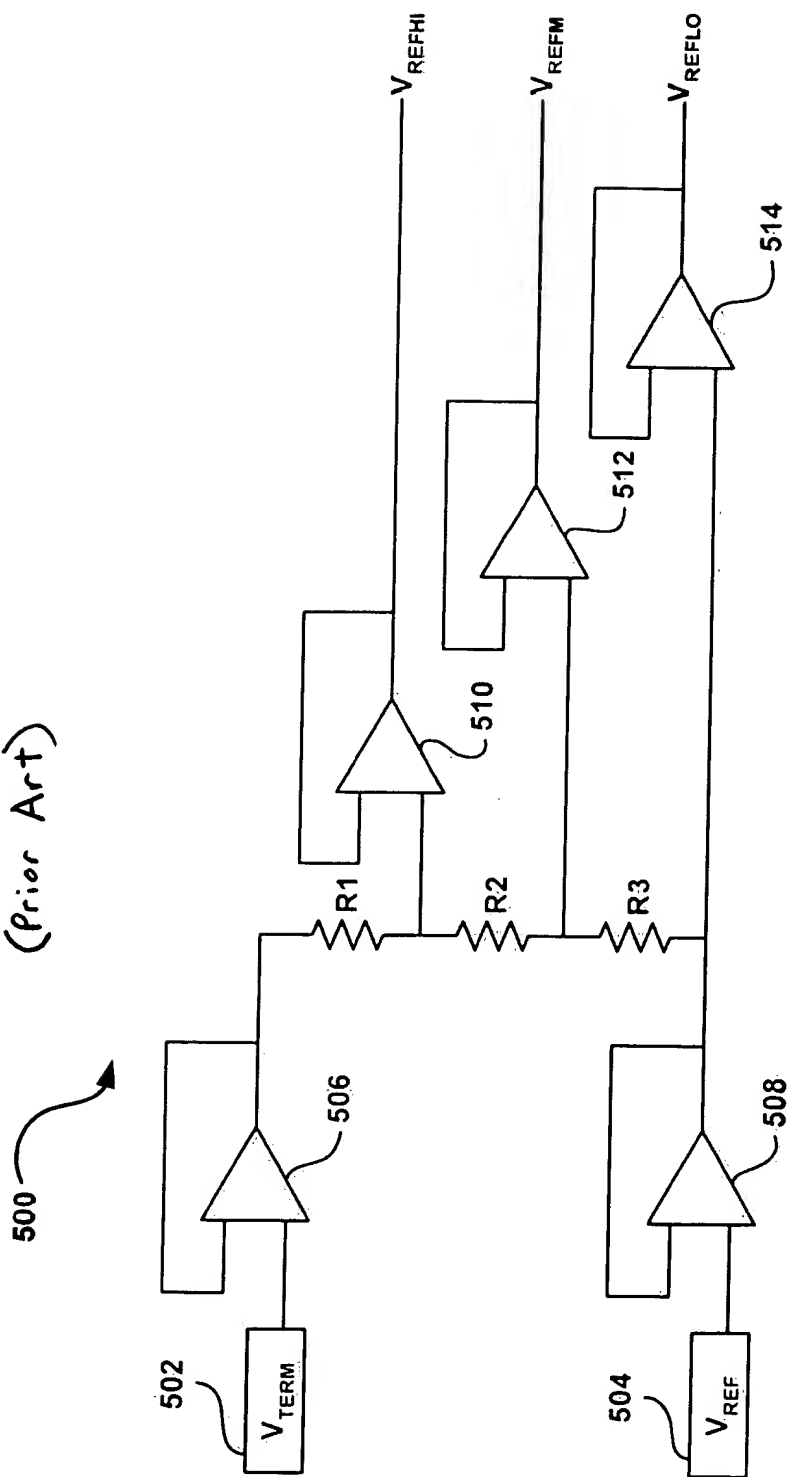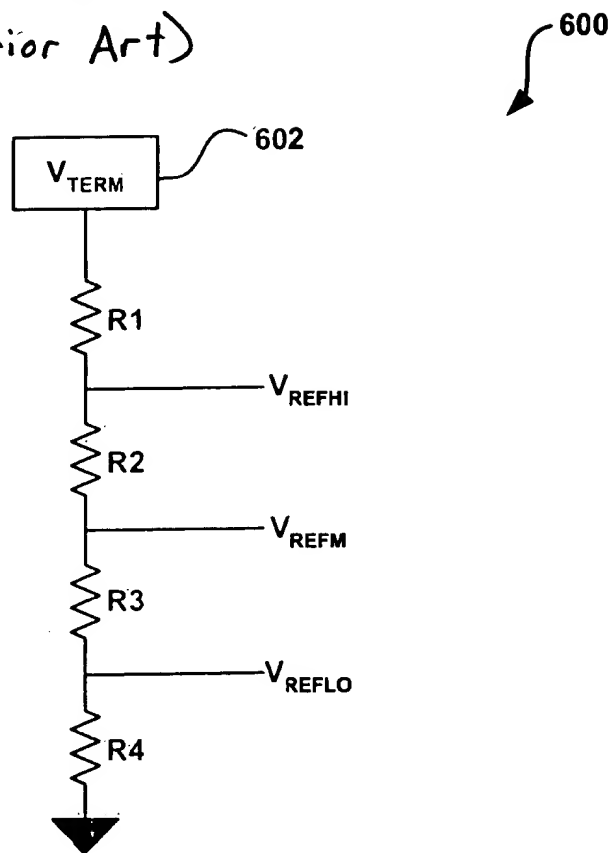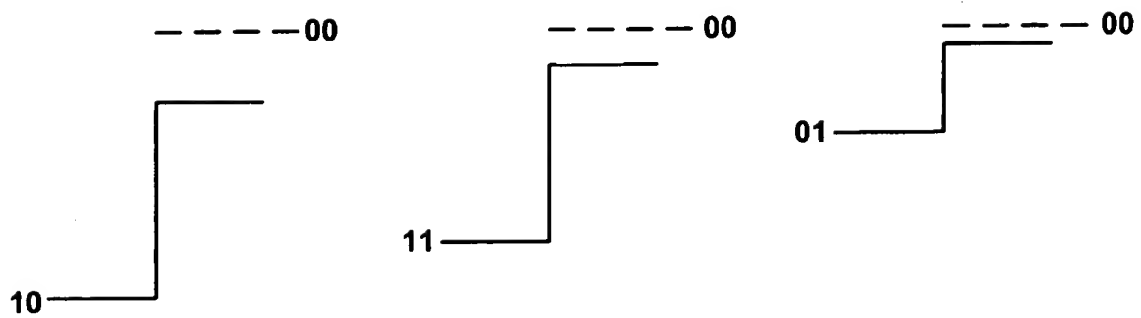
FIGURE 9

FIGURE 13

FIGURE 15

1100